Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A host controller for use in a bus communication device having a host microprocessor and a system memory, the host controller comprising:

a first interface for direct connection to a memory bus which connects the host microprocessor and the system memory, such that the host controller is adapted to act only as a slave on the memory bus;

an internal memory configured into at least two distinct sections to store a plurality of transfer-based transfer descriptors including a first section configured to store a plurality of transfer-based transfer descriptor headers, and a second section configured to store a plurality of transfer-based transfer descriptor payloads, the respective transfer-based transfer descriptors received through the first interface, said internal memory having a plurality of transfer-based transfer descriptor header and transfer-based transfer descriptor payload locations mapped in the host microprocessor, said first section of the internal memory is sub-divided into two sub-parts, and is adapted to consecutively store transfer descriptor headers relating to periodic transfers in a first subpart, and to consecutively store transfer descriptor headers relating to asynchronous transfers in a second sub-part; and

a second interface, for connection to an external bus,

wherein the host controller is adapted to:

execute stored transfer-based transfer descriptors;

update the content of the stored transfer-based transfer descriptors on execution; and

copy the updated stored transfer-based transfer descriptors to the system memory.

2. (Original) A host controller as claimed in claim 1, wherein the internal memory is a dual-port RAM.

3. (Original) A host controller as claimed in claim 1, wherein the internal memory is a single-port RAM, and the host controller further comprises an arbiter to allow data to be written to and read from the RAM essentially simultaneously.

4-5. (Canceled)

6. (Currently Amended) A host controller as claimed in claim ~~5~~1, wherein the host controller is adapted to scan the first sub-part of the internal memory once in each micro-frame, and is adapted to scan the second sub-part continuously throughout each micro-frame.

7. (Original) A host controller as claimed in claim 1, wherein the host controller is a USB host controller and the second interface is a USB bus interface.

8. (Original) A host controller as claimed in claim 1, wherein the internal memory is adapted to store multiple micro-frames of transfer descriptors, and to execute the stored transfer descriptors without intervention from the host microprocessor.

9. (Original) A host controller as claimed in claim 8, wherein each of the multiple micro-frames of transfer descriptors may store payload data relating to one or more of isochronous, interrupt and bulk data transfers.

10. (Currently Amended) A bus communication device, comprising:
a host microprocessor;
a system memory;

a memory bus, which connects the host microprocessor and the system memory; and

a host controller, wherein the host microprocessor is adapted to form transfer-based transfer descriptors, and write the transfer-based transfer descriptors to the system memory and to the host controller, and wherein the host controller comprises:

a first interface for direct connection to the memory bus, such that the host controller is adapted to act only as a slave on the memory bus;

an internal memory, for storing a plurality of transfer-based transfer descriptors, the internal memory having a first section adapted to consecutively store transfer descriptor headers and a second section adapted to consecutively store transfer descriptor payloads, the first section sub-divided into a first subpart adapted to consecutively store transfer descriptor headers relating to periodic transfers and a second subpart adapted to consecutively store transfer descriptor headers relating to asynchronous transfers, the transfer descriptors ~~including header and payload,~~ received through the first interface, said internal memory having a plurality of header and payload transfer descriptor locations mapped in the host microprocessor; and

a second interface, for connection to an external bus,

wherein the host controller is adapted to:

execute stored transfer-based transfer descriptors;

update the content of the stored transfer-based transfer descriptors on execution; and

copy the updated stored transfer-based transfer descriptors to the system memory.

11. (Original) A bus communication device as in claim 10, wherein the second interface for the host controller is a USB bus interface, and the bus communication device is adapted to act as a USB host.

12. (Original) A bus communication device as claimed in claim 10, wherein the host microprocessor is adapted to write a plurality of micro-frames of transfer descriptors to the system memory and to the host controller, and the host controller is adapted to execute the plurality of micro-frames of transfer descriptors without intervention from the host microprocessor.

13. (Previously Presented) A host controller as claimed in claim 1, wherein the first interface comprises:

a memory mapped input/output;

a memory management unit; and

a slave direct memory access (DMA) controller.

14. (Previously Presented) A host controller as claimed in claim 1, wherein the first interface comprises registers.

15. (Previously Presented) A host controller as claimed in claim 14, further comprising a logic unit, wherein the logic unit comprises the second interface.

16. (Previously Presented) A host controller as claimed in claim 15, further comprising an internal bus coupled between the registers and the logic unit, wherein the internal bus is configured to carry control signals from the registers to the logic unit.

17. (Previously Presented) A host controller as claimed in claim 1, further comprising an external connection to the first interface, wherein the external connection is configured to carry control and interrupt signals.

18. (Previously Presented) A bus communication device as claimed in claim 10, wherein the host controller further comprises:

a memory mapped input/output;

a memory management unit;

a slave direct memory access (DMA) controller; and

registers

19. (Previously Presented) A bus communication device as claimed in claim 18, wherein the host controller further comprises:

a logic unit, wherein the logic unit comprises the second interface; and

an internal bus coupled between the registers and the logic unit, wherein the internal bus configured to carry control signals from the registers to the logic unit.

20. (Previously Presented) A bus communication device as claimed in claim 10, wherein the host controller further comprises an external connection to the first interface, wherein the external connection is configured to carry control and interrupt signals.

21. (Previously Presented) The host controller as claimed in claim 1 wherein the host controller is further configured to respond to memory transactions scheduled by the host microprocessor.

22. (Previously Presented) The bus communication device as claimed in claim 10, wherein the plurality of locations of the internal memory mapped to the system memory are configured for access by the host microprocessor when the host microprocessor addresses the mapped addresses of the system memory.

23. (Currently Amended) A method of executing bus transactions with a host controller comprising:

configuring the host controller as a slave on a memory bus, the memory bus directly connected to the host controller, a host microprocessor, and a system memory;

configuring ~~header and payload transfer based~~ a block of dedicated transfer descriptor header address space of an internal memory to be mappable in the host microprocessor, said address space accessible via the memory bus;

configuring a block of dedicated transfer descriptor payload address space of an internal memory to be mappable in the host microprocessor,

wherein said address space accessible via the memory bus, wherein the block of dedicated transfer descriptor header address space is separate from the block of dedicated transfer descriptor payload address space, and wherein the block of dedicated transfer descriptor header address space is sub-divided into a first subpart adapted to consecutively store transfer descriptor headers relating to periodic transfers and a second subpart adapted to consecutively store transfer descriptor headers relating to asynchronous transfers;

~~configuring the internal memory to store a plurality of header and payload transfer based transfer descriptors received via the memory bus;~~

reading transfer-based transfer descriptors from the internal memory;

executing the transfer-based transfer descriptors; and

updating the content of the transfer-based transfer descriptors on execution.